Amendments to the Specification:

Please replace the paragraph beginning on page 3, line 7 with the following rewritten paragraphs:

~~Fig. 3 is a timing and block diagram for color difference readout;~~

--Fig. 3a is a block diagram for color difference readout;--

--Fig. 3b is a timing diagram of Fig. 3a;--

Please replace the paragraphs beginning on page 3, line 13 with the following rewritten paragraphs:

~~Fig. 6a is a first timing and block diagram for operation of the sensor shown in Fig. 2;~~

~~Fig. 6b is a timing and block diagram for operation of a second embodiment of the present invention;~~

--Fig. 6a is a block diagram for operation of the sensor shown in Fig. 2;--

--Fig. 6b first timing diagram of Fig. 6a;--

--Fig. 6c is a block diagram for operation of a second embodiment of the present invention;--

--Fig. 6d is a timing diagram of Fig. 6c;--

--~~Fig. 6e~~ Fig. 6e is an operational block diagram for adjacent sample averaging operation of the sensor shown in Fig. 5a;--

--~~Fig. 6d~~ Fig. 6f is a second operational block diagram for two row readout operation of the sensor shown in Fig. 5a;--

Please replace the paragraph beginning on page 5, line 21 with the following rewritten paragraph:

--Still referring to the architecture in Fig. 2, the dashed lines with arrows within each column indicate which direction or bank of column circuits that the specific pixel is sampled and held in for a first preferred embodiment of the present invention. In this first configuration, all pixels of a particular color in a row are sent to a common column circuit bank. For example, all red pixels in odd ~~even~~ rows are sent to column circuit bank 2, and all green pixels in odd ~~even~~ rows are sent to column circuit bank 1. In even ~~odd~~ rows, all blue pixels are sent to column circuit bank 2 and all green pixels are sent to column circuit bank 1.

In this manner, the green color plane would go through a single ASP chain 110 and ADC 120, while red and blue would go through the other ASP chain 110 and ADC 120. As a result, no offset or gain mismatch would occur between green pixels in the green-red row (Gr), and green pixels in the green-blue row (Gb). This is accomplished by timing of the pixel output multiplexer 160 ~~130~~. This specific timing for this example is shown in ~~Fig. 6a~~ Figs. 6a and 6b. The signals Bank1_e and Bank1_o determine if the even and odd pixels respectively in a given row are sent to column circuit bank 1. Bank2_e and Bank2_o serve the same purpose for column circuit bank 2. For odd rows, Bank1_e is high, Bank1_o is low, Bank2_e is low and Bank2_o is high. For even rows, Bank1_e is low, Bank1_o is high, Bank2_e is high and Bank2_o is low. This color plane separation approach enabled by the present invention can mitigate the GNU issue. In general, the timing of the pixel output multiplexers can be used to send any pixel to either or both of the associated column sample and hold circuits.--

Please replace the paragraph beginning on page 6, line 21 with the following rewritten paragraph:

--In another configuration of this same architecture, a color difference readout can be provided. The color difference readout operation will be described using the four transistor active pixel shown in Fig. 4, although the other pixel architectures can be used without departing from the scope of the invention. Referring to the sensor block diagram and timing diagram in ~~Fig. 3~~ Figs. 3a and 3b, color difference readout is accomplished in the following manner. Referring to both ~~Figs. 3~~ Figs. 3a, 3b, and 4, after integration is completed, readout of the row 1 commences after reset of the floating diffusions 190 of the pixels in that row, (a green-red row in this example). The reset level of the floating diffusion 190 in the green pixel is then stored as the reference level in one column circuit bank 80. This is referred to as Resetg. Next the signal in the photodiode 170 is transferred to the floating diffusion 190 for all pixels in the row. The signal level on the floating diffusion 190 in the red pixels is now stored as the reference level in the second column circuit bank 80. This voltage level stored is R + Resetr. Next the signal level of the floating diffusion 190 in the green pixel is stored as the signal level in both column circuit banks. This is G + Resetg. Readout of the stored signal now commences. One column bank 80 produces a true correlated double sample readout of the green signal level as shown in equation 1.--

Please replace the paragraph beginning on page 7, line 16 with the following rewritten paragraph:

--Another embodiment of the selectable dual channel sensor architecture of the present invention is shown in ~~Fig. 6b~~ Figs. 6c and 6d. The analog multiplexers (160 in the previous Figures) are eliminated and separate control of sample and hold signals for each bank are provided. These signals are labeled SHS_e and SHS_o for sample and hold signal even and odd respectively, and SHR_e and SHR_o for sample and hold reference even and odd respectively. These are provided separately for column circuit banks 1 and 2 (80) and denoted in ~~Fig. 6b~~ Figs. 6c and 6d accordingly. The analogous timing for ~~Fig. 6a~~ Figs. 6a and 6b with this architecture is shown in ~~Fig. 6b~~ Figs. 6c and 6d. In general the timing of the bank sample and hold signals can be used to send any pixel to either or both of the associated column sample and hold circuits 150.--

Please replace the paragraphs beginning on page 8, line 6 with the following rewritten paragraphs:

--The same color plane separation can be accomplished with the two channel sensor architectures of Figs. 5a and 5b in a similar manner as described for the sensor architecture of ~~Figs 2 and 3~~ Figs. 2, 3a, and 3b. The sensor architectures of Figs. 5a and 5b provide an additional capability over that already described. Because the column sample and hold circuits 150 are built at the pixel pitch, the two channel architecture can effectively store and readout two samples of each pixel in a single row of image data simultaneously. By timing the pixel output multiplexer 160, two samples of the pixel value in each row of sensor data can be stored with the color planes separated for efficient adjacent sample averaging. This is shown in ~~Fig. 6e~~ Fig. 6e. Again the operation is described in the context of the pixel shown in Fig. 4 in a rolling shutter mode. Other pixel architectures and modes of operations can be used without departing from the scope of the invention. After integration ends, sample and hold of row 0, an odd ~~even~~ row, commences. Each Gr pixel signal level is stored in two adjacent column locations of column circuit bank 1 (80) by using the pixel output multiplexer 160 to connect the Gr pixel output to both of the associated column sample and hold circuits 150 in bank 1 (80). Each of the G pixels stored in the respective column sample and hold circuit is labeled as G0X, where 0 denotes

row zero and X denotes the column number in that row. As shown in ~~Fig. 6e~~ Fig. 6e each G pixel in the row gets stored in two adjacent column locations in column circuit bank 1 (80). Similarly each of the R signal values in row 0 is sampled and held in two adjacent column sample and hold circuits 150 in bank 2 (80). Now the two banks (80) can be read out in parallel and the two adjacent stored signals from a single pixel can be averaged to create a lower noise value. The average is most easily accomplished in the digital domain after analog to digital conversion. The process is repeated for the next row, an even ~~odd~~ row, where two samples of Gb are stored in bank 1 (80), and two adjacent samples for each B are stored in bank 2 (80). In general, this approach can be employed with n-sample and holds connected to a single pixel to provide n-sample averaging.--

--The same color plane separation afforded by the two channel sensor architecture of ~~Figs. 2 and 6b~~ Figs. 2, 6c, and 6d can also be accomplished with the two channel sensor architecture of Figs. 5a and 5b by storage and readout of two rows in parallel. Referring to ~~Fig. 6d~~ Fig. 6f, after integration ends sample and hold of row 0, an odd ~~even~~ row, commences. Each Gr pixel signal level is stored in even column locations of column circuit bank 1 (80) by using the pixel output multiplexer 160 to connect the Gr pixel output to the even column locations of the associated column sample and hold circuits 150 in bank 1 (80). Similarly each of the R pixel signal values is sampled and held in the odd column sample and hold circuits 150 in bank 2 (80). Next row 1, an even ~~odd~~ row is sampled and held. Each Gb pixel signal level is stored in odd column locations of column circuit bank 1 (80) by using the pixel output multiplexer 160 to connect the Gb pixel output to odd column locations of the associated column sample and hold circuits 150 in bank 1 (80). Similarly each of the B pixel signal values is sampled and held in the even column sample and hold circuits 150 in bank 2 (80). Now the two banks (80) can be read out in parallel. This is shown in ~~Fig. 6d~~ Fig. 6f by placement of specific R, G and B pixels in the column circuits with a value of Cxy, where C denotes the color, x denotes the row and y denotes the column. For example B10 is the blue pixel in row 1 and column 0. This process is repeated for each group of two rows in the array. By storage and readout in this manner, a 2x2 region of the array is always available in the digital domain and this can be utilized for on-chip pipelined color processing.--

Please replace the paragraph beginning on page 12, line 14 with the following rewritten paragraph:

--This same charge domain binning and voltage or digital domain adjacent sample averaging can be utilized with the sensor architecture of Figs. 5a and 5b. The sensor architectures of Fig. 5a and 5b provide an additional capability over that already described. Because the column sample and hold circuits 150 provided at the pixel pitch, the two channel architecture can effectively store two rows of image data simultaneously. By timing the pixel output multiplexer two rows of sensor data can be stored with the color planes separated for efficient adjacent sample averaging. Referring to Figs. 5a, 7, and ~~6e~~ 6e, it follows that R', B', Gr' and Gb' pixel values can be stored in the column circuit banks 80 as shown in Fig. 9, where R', B', Gr' and Gb' are the charge domain binned values for the paxel. These are denoted in Fig. 9 as the sum of two pixel values shown in each column circuit 150 location. Gr' and Gb' are stored in Bank 1 (80), and R' and B' are stored in bank 2 (80) as previously described. Now adjacent values of each color can be averaged in a pipelined manner as the sensor is read out.--